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Stability Comparison of 6T and 8T SRAM Cell

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**ABSTRACT** -In the modern world as the technology is improving, there is a strong demand to design the SRAM cell for High speed application, Mainly the SRAM cell speed is depending on their (SNM) static noise margin and this is the one of the main parameter to design a memory cell, the static noise margin is going to affect the read margin and write margin.the SNM plays a vital role in stability of SRAM Cell. The analysis of SRAM read/write margin is essential for high speed SRAMs the tool used for simulation purpose is IC Station by Mentor Graphics using 350nm technology compared with 180nm

KEYWORD: SRAM, Read noise margin, write margin, Static noise margin, Cell Ratio, Pull up Ratio

### I. INTRODUCTION

An SRAM (Static Random Access Memory) cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" it is base on the read noise margin (RNM) and the write noise margin (WNM) this both a margin is depending on the static noise margin (SNM).Principle: The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors (Figure 1). When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop the flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile (i.e., the data is lost when the power is removed). The noise margin ratio for low threshold voltage (Vth) design is, In a 6T SRAM cell using low Vth devices ( |Vth |= 0.19 V) shows a comparable read static noise margin (RSNM), 41% improvement in σRSNM, 84% improvement in write static noise margin (WSNM), and 67% improvement in σWSNM as compared with the case using higher Vth devices (|Vth| = 0.49 V) [5] Transistor mismatch will degrades the RSNM and the SRAM current Cell the transistor mismatch, we performed Monte Carlo simulations for Read SNM and Icell under the condition of  $\sigma$ th=Vth/10, The worst normalized Read SNM and normalized Icell values are, respectively, 0.60 and 0.72 for oth=Vth/5 values are 0.20 and 0.44 in the 7T SRAM Cell just add one transistor for loop cutting making it possible to reduce area overhead from 30% to 13% [4]. During Read operation in 6T SRAM cell, the fundamental stability problem occurs. In order to reduce leakage power consumption, pre-charge voltage for bit-lines is kept much lower than the cell supply voltage. When the transistors are turned on, the '0' logic node is pulled up to a poor '0' level and the '1' logic node is pulled down to a poor '1' level; this may lead to flip the cell data.



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### Figure 1. SRAM CELL

#### **II. STATIC NOISE MARGIN**

In this section, first we introduce Static noise margin of the SRAM cell depends on the cell ratio (CR), supply voltage and also pull up ratio. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage [1].Driver transistor is responsible for 70 % value of the SNM. [6]



#### Figure 2. 6T SRAM CELL

The read static-noise-margin of the proposed circuit is thereby enhanced by 2X as compared to a conventional six-transistor (6T) SRAM cell. Thereby reducing the leakage power consumption by 22.9% Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation. Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation. The basic circuit of SRAM cell is given below [1]



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### **III. PROPOSED CELL STRUCTURE OF 8T SRAM**

In the Proposed Cell Structure Of 8t SRAM cell, There are three MOSFETs are introduced to separate the read and write current paths and to avoid the accidental flipping of cell during read operation. This results in significantly large SNM during Read operation. The Read operation in 8T cell is performed by using MOSFETs M6, M7 and M8.Bit-line is pre-charged to logic '1' for successful read operation.

#### **3.1 READ OPERATION / MARGIN**

Node 'Qbar' is connected to the gates of M7 and M8 transistors. When transistor M6 is turned 'ON' using Read\_Word\_Line, current starts flowing in and out of the read circuit Sense amplifier is used to read the cell data by sensing the Bit-Line voltage fluctuation. The amplifier detects the voltage difference of its inputs. For read '1'operation, the initial states of Q and Qbar are assumed to be '1' and '0' respectively. As 'Qbar' node stores '0' logic, on turning 'ON' M6 transistor, it enables the M8 (PMOS) transistor which in turn charges the Bit Line through M8 and M6. The sense amplifier detects the bit swing and output '1' is obtained[8].During read '0' operation Read Word Line enables the M6 and as 'Qbar' node stores logic '1', it turns on M7 (NMOS) which discharges the Bit-Line through M7 and M6 and logic '0' is obtained at the output.

We calculate the read margin based on the transistor's current model. Experimental results show that the read margin accurately captures the SRAM's read stability as a function of the transistor's threshold voltage and the power supply voltage variations. Observed that both read margin and SNM are proportional with respect to the CR and we observed that both write margin and SNM are proportional with respect to the PR [1].



Figure 3. Proposed 8t SRAM Cell

#### **3.2 WRITE OPERATION/ MARGIN**

In this cell structure of 8T SRAM cell only single bit-line is used for read and writes operation as compared to conventional 6T SRAM.During write '1' operation, enabling the Write Word Line will turn on M5 transistor. As the Bit Line is charged to logic '1' for write '1' operation, the 'Q' node starts charging and turns on M1 which leads to flip 'Qbar' node to logic '0'. Now 'Qbar' node helps enabling the M4 which facilitates writing logic '1' at 'Q' node. On the other hand, during write '0' operation, the Bit Line is charged to logic '0' and M5 turns on, by enabling Write Word Line signal. The 'Q' node starts discharging and turns on M2 which in turn flips 'Qbar' node to logic '1'. Now 'Qbar' helps turning M3 on, which facilitates discharging 'Q' node properly, and consequently logic '0' is obtained at 'Q' node.



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Write margin is defined as the minimum bit line voltage required flipping the state of an SRAM cell [1]. The write margin value and variation is a function of the cell design, SRAM array size and process variation. First we calculated write margin by the existing BL sweeping method then we compared that with Static Noise Margin. Write margin is directly proportional to the pull up ratio. Write margin increases with the increases value of the pull up ratio [5]. So carefully you have to design SRAM cell inverters before calculating the write margin of SRAM cell during write operation. Pull up ratio also fully depends on the size of the transistor.

#### IV ANALYSIS

The simulation results of 8T SRAM cell are analyzed and compared with the conventional 6T SRAM cell for Cell ratio, Pull up Ratio, variations and corresponding SNM and power dissipation is calculated in 350 nm technology with supply voltage of 2.5V.

#### 4.1 CELL RATIO VS SNM

In this section, static noise margin is calculated by varying the cell ratio of transistors. Cell ratio is the ratio of sizes of driver transistor to the access transistor. As the cell ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell.

Cell Ratio (CR)= (W1/L1) / (W5/L5) (During Read Operation)

The static noise margin of 8T SRAM cell calculated by varying the cell ratio and comparison with 6T is done. Results show that SNM i.e. stability of 8T SRAM cell is higher than the 6T SRAM cell as it uses a separate word line for read operation In Figure 3, The profile of the Static noise margin for both 8T SRAM and 6T SRAM cells are shown for different cell ratios. Here the 8T SRAM cell has better SNM than 6T cell.

#### 4.2 PULL UP RATIO VS SNM

In this section, static noise margin is calculated by varying the Pull up ratio of transistors. Pull up ratio is the ratio of sizes of load transistor to the access transistor. As the Pull up ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell. SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased



Figure 4 Calculated SNM for both cells



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. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS devices. Changing the Cell Ratio, we got different speed of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, for hence current also increases. As current is an increase, the speed of the SRAM cell also increases. The static noise margin is a side of Maximum Square drawn between the inverter characteristics [2]





#### **V. CONCLUSION**

The study of this paper, the stability analysis for various parameters such as read margin and write margin for 8T SRAM cell has been done. Also, the results are compared with conventional 6T SRAM cell. From the above analysis it can be concluded that Static Noise Margin (SNM) of 8T SRAM cell is better than the conventional 6T SRAM cell. These analysis are very useful for future research work on 6T or 8T SRAM cell as using these we can clarify the stability of memory cells. Using noise margin of memory cell it is easier to configure a new SRAM cell with higher stability and lower noise

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