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# Stability Comparison of 6T and 8T SRAM Cell

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**ABSTRACT** -In the modern world as the technology is improving, there is a strong demand to design the SRAM cell for High speed application, Mainly the SRAM cell speed is depending on their (SNM) static noise margin and this is the one of the main parameter to design a memory cell, the static noise margin is going to affect the read margin and write margin.the SNM plays a vital role in stability of SRAM Cell. The analysis of SRAM read/write margin is essential for high speed SRAMs the tool used for simulation purpose is IC Station by Mentor Graphics using 350nm technology compared with 180nm

**KEYWORD:** SRAM, Read noise margin, write margin, Static noise margin, Cell Ratio, Pull up Ratio

### I. INTRODUCTION

An SRAM (Static Random Access Memory) cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" it is base on the read noise margin (RNM) and the write noise margin (WNM) this both a margin is depending on the static noise margin (SNM).Principle: The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors (**Figure 1**). When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop the flip-flop needs the power supply to keep the information. The data in an SRAM cell is volatile (i.e., the data is lost when the power is removed). The noise margin ratio for low threshold voltage ( $V_{th}$ ) design is, In a 6T SRAM cell using low  $V_{th}$  devices ( $|V_{th}| = 0.19$  V) shows a comparable read static noise margin (RSNM), 41% improvement in  $\sigma_{RSNM}$ , 84% improvement in write static noise margin (WSNM),and 67% improvement in  $\sigma_{WSNM}$  as compared with the case using higher  $V_{th}$  devices ( $|V_{th}| = 0.49$  V) [5] Transistor mismatch will degrades the RSNM and the SRAM current Cell the transistor mismatch, we performed Monte Carlo simulations for Read SNM and Icell under the condition of  $\sigma_{th}=V_{th}/10$ , The worst normalized Read SNM and normalized Icell values are, respectively, 0.60 and 0.72 for  $\sigma_{th}=V_{th}/5$  values are 0.20 and 0.44 in the 7T SRAM Cell just add one transistor for loop cutting making it possible to reduce area overhead from 30% to 13% [4]. During Read operation in 6T SRAM cell, the fundamental stability problem occurs. In order to reduce leakage power consumption, pre-charge voltage for bit-lines is kept much lower than the cell supply voltage. When the transistors are turned on, the '0' logic node is pulled up to a poor '0' level and the '1' logic node is pulled down to a poor '1' level; this may lead to flip the cell data.





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Write margin is defined as the minimum bit line voltage required flipping the state of an SRAM cell [1]. The write margin value and variation is a function of the cell design, SRAM array size and process variation. First we calculated write margin by the existing BL sweeping method then we compared that with Static Noise Margin. Write margin is directly proportional to the pull up ratio. Write margin increases with the increases value of the pull up ratio [5]. So carefully you have to design SRAM cell inverters before calculating the write margin of SRAM cell during write operation. Pull up ratio also fully depends on the size of the transistor.

## IV ANALYSIS

The simulation results of 8T SRAM cell are analyzed and compared with the conventional 6T SRAM cell for Cell ratio, Pull up Ratio, variations and corresponding SNM and power dissipation is calculated in 350 nm technology with supply voltage of 2.5V.

### 4.1 CELL RATIO VS SNM

In this section, static noise margin is calculated by varying the cell ratio of transistors. Cell ratio is the ratio of sizes of driver transistor to the access transistor. As the cell ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell.

$$\text{Cell Ratio (CR)} = (W1/L1) / (W5/L5) \text{ (During Read Operation)}$$

The static noise margin of 8T SRAM cell calculated by varying the cell ratio and comparison with 6T is done. Results show that SNM i.e. stability of 8T SRAM cell is higher than the 6T SRAM cell as it uses a separate word line for read operation. In Figure 3, The profile of the Static noise margin for both 8T SRAM and 6T SRAM cells are shown for different cell ratios. Here the 8T SRAM cell has better SNM than 6T cell.

### 4.2 PULL UP RATIO VS SNM

In this section, static noise margin is calculated by varying the Pull up ratio of transistors. Pull up ratio is the ratio of sizes of load transistor to the access transistor. As the Pull up ratio increases by increasing the size of driver transistor, Static noise margin of memory cell also increases which results in increase of current in a memory cell. SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased

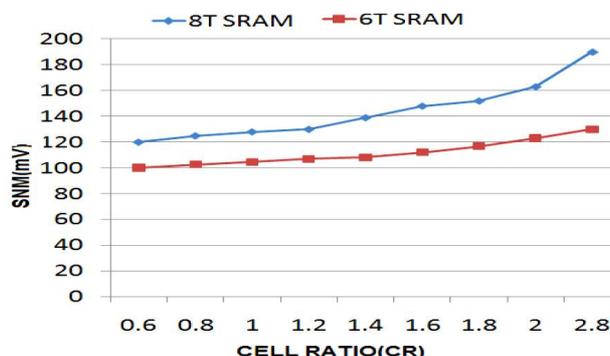


Figure 4 Calculated SNM for both cells

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. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS devices. Changing the Cell Ratio, we got different speed of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, for hence current also increases. As current is an increase, the speed of the SRAM cell also increases. The static noise margin is a side of Maximum Square drawn between the inverter characteristics [2]

$$\text{Pull up Ratio (PR)} = (W_4/L_4)/(W_6/L_6) \text{ (During Write Operation)}$$

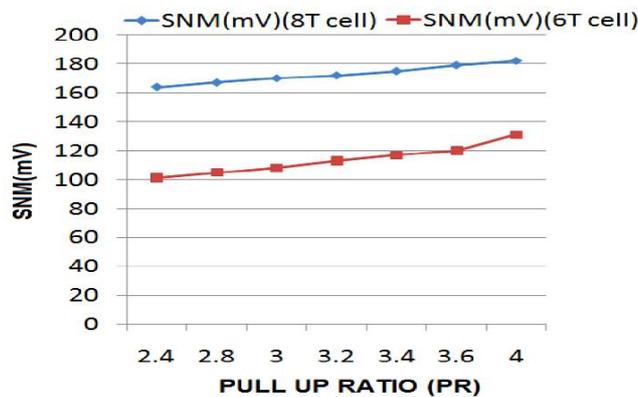


Figure 5 SNM by varying Pull up ratio for both cells

### V. CONCLUSION

The study of this paper, the stability analysis for various parameters such as read margin and write margin for 8T SRAM cell has been done. Also, the results are compared with conventional 6T SRAM cell. From the above analysis it can be concluded that Static Noise Margin (SNM) of 8T SRAM cell is better than the conventional 6T SRAM cell. These analysis are very useful for future research work on 6T or 8T SRAM cell as using these we can clarify the stability of memory cells. Using noise margin of memory cell it is easier to configure a new SRAM cell with higher stability and lower noise

### REFERENCES

- [1] Static Noise Margin Analysis of SRAM Cell for High Speed Application IJCSI International Journal of Computer Science Issues, Vol. 7, Issue 5, September 2010 ISSN (Online): 1694-0814 [www.IJCSI.org](http://www.IJCSI.org)
- [2] COMPARATIVE PARAMETRIC ANALYSIS FOR STABILITY OF 6T AND 8T SRAM CELL Debasis Mukherjee<sup>1</sup>, Hemanta Kr. Mondal<sup>2</sup> and B.V.R. Reddy<sup>3</sup> Manpreet Kaur<sup>1</sup>, Ravi Kumar Sharma<sup>2</sup> 1Lovely Professional University, Jalandhar, Punjab, India 2Vivekanand Institute of Technology, Jaipur, Rajasthan, India International Journal of Advances in Engineering & Technology, Nov. 2012. ©IJAET ISSN: 2231-1963
- [3] Low Power 8T SRAM Cell Design For High Stability Video Applications Maisagalla Gopal & Balwinder Raj Department of ECE, National Institute of Technology Jalandhar, Punjab ISSN (PRINT): 2320 – 8945, Volume -1, Issue -5, 2013
- [4] A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications Koichi Takeda, Yasuhiko Hagihara, Yoshiharu Aimoto, Masahiro Nomura, Member, IEEE, Yoetsu Nakazawa, Toshio Ishii, and Hiroyuki Kobatake IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 1, JANUARY 2006
- [5] Threshold Voltage Design of UTB SOI SRAM With Improved Stability/Variability for Ultralow Voltage Near Subthreshold Operation Vita Pi-Ho Hu, Member, IEEE, Ming-Long Fan, Student Member, IEEE, Pin Su, Member, IEEE, and Ching-Te Chuang, Fellow, IEEE. IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 12, NO 4, JULY 2013, 1536-125X/\$31.00 © 2013 IEEE
- [6] Characterization of a Novel Nine-Transistor SRAM Cell Zhiyu Liu and Volkan Kursun IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 16, NO 4, APRIL 2008
- [7] Comparison of SRAM Cells for 10-nm SOI FinFETs Under Process and Environmental Variations Zoran Jakšić and Ramon Canal IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 1, JANUARY 2013

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- [8] Increase in Read Noise Margin of Single-Bit-Line SRAM Using Adiabatic Change of Word Line Voltage Shunji Nakata, Hiroki Hanazono, Hiroshi Makino, Hiroki Morimura, Masayuki Miyama, and Yoshio Matsuda IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1063-8210/\$31.00 © 2013 IEEE
- [9] Stability Estimation of a 6T-SRAM Cell Using a Nonlinear Regression Henry Park, Student Member, IEEE, and Chih-Kong Ken Yang, Fellow, IEEE IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1063-8210/\$31.00 © 2013 IEEE
- [10] New Low-Power and High-Speed 9T SRAM cell in Dynamic Domino Logic R.Uma1, Alok Katiyar2, K.Anusudha2, P.Dhavachelvan1 1Department of Computer Science, School of Engineering 2Department of Electronics, School of Engineering Pondicherry University Pondicherry ISSN : 0975-4024 Vol 5 No 2 Apr-May 2013
- [11] D. Ho, K. Iniewski, S. Kasnavi, A. Ivanov, and S. Natarajan, "Ultra-low power 90 nm 6T SRAM cell for wireless sensor network application," in Proc. IEEE Int. Symp. Circuits Syst., May 2006, pp. 4131-4134.
- [12] S. R. Singh and K. Moez, "Ultra-low leakage 90 nm content addressable memory design for wireless sensor network applications," in Proc. IEEE Int. Midwest Symp. Circuits Syst., Aug. 2009, pp. 1191-1194.
- [13] S. Nakata, H. Suzuki, H. Makino, S. Mutoh, M. Miyama, and Y. Matsuda, "Increasing static noise margin of single-bit-line SRAM by lowering bit-line voltage during reading," in Proc. IEEE Int. Midwest Symp. Circuits Syst., Aug. 2011, pp. 1-4.
- [14] J. C. Kao, W. H. Ma, V. S. Sathe, and M. Papaefthymiou, "Energy efficient low-latency 600 MHz FIR with high-overdrive charge-recovery logic," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 6, pp. 977-988, Jun. 2012.

## BIOGRAPHY



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